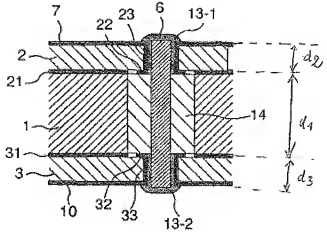
Remarks:

Applicant has read and considered the Office Action dated March 2, 2010 and the references cited therein. Claims 1, 3, 8, 10-11 and 16 have been amended. Claim 5 was previously cancelled. Claims 1-4 and 6-16 are currently pending. Reconsideration is hereby requested.

Although it is believed that the expression "antenna plate" as used in the context of the present application clearly refers to an antenna substrate which is not electrically conductive, solely to avoid confusion and provide clarification, the expression "antenna plate" in claim 1 has been replaced with "antenna printed circuit board". In Sekine the solder material 13-2 is in contact with the dielectric material 14 of the coaxial line. This dielectric material 14 of the coaxial line, is clearly not a printed circuit board.

In the Response to Arguments, the Office Action states that Applicant has not provided convincing arguments as to why it is not possible to make the length of the central conductor in Sekine smaller than a quarter-wavelength for typical signals processed in high frequency applications, because the central conductor is extending through three different substrates. To demonstrate that it is not possible to make the length of the central conductor in Sekine smaller than a quarter wavelength, Figure 5 of Sekine is inserted below with the thicknesses of the different layers labelled. These thicknesses are estimated to have the following values by a person of ordinary skill in the art:

FIG.5



$d_1 \approx 1.5 - 2$ mm

$d_2 \approx 0.5$ mm

$d_3 \approx 0.5$ mm

Applicant notes that layer 1 is a base plate and not a dielectric. Such a base plate is made of a metal and has a typical thickness of 1.5 to 2 mm, see also column 6, line 13 of Sekine. Layers 1 and 2 are substrates formed of a dielectric. Such substrates have a typical thickness of 0.5 mm.

In the present invention a thin printed circuit board is used typically having a thickness of about 0.25 mm. This is ten times thinner than what is disclosed in Sekine and therefore many times smaller. In addition, this provides for accurate results for processing high frequency signals above 10 GHz. Claim 1 now recites a device for processing high frequency signals above 10 GHz and that the length of the passage is to be many times smaller than a quarter

wavelength of the signal to be processed by the antenna. Support for this language is found in the specification and claims are originally filed and no new matter has been added.

The Office Action notes that the claim language refers only to a metal passage, which can encompass a coaxial line. However, claim 1 on file refers to a metal passage through the antenna plate that transposes into a bond pad against the antenna plate on the second side. In Sekine, even if the central conductor of the coaxial line is considered to be a metal passage, such a metal passage does not transpose into a bond pad against the second side of the antenna plate. The solder 13-2 is clearly not a pad. However, to eliminate any confusion in claim 1, the expression "a metal passage through the antenna plate which transposes into a bond pad against the antenna plate on the second side" has been replaced with "a metal passage through a hole in the antenna printed circuit board, the hole defining a wall, said metal passage being in direct contact with the wall of said hole and said metal passage transposing into a bond pad against and in direct contact with the second side of the antenna printed circuit board".

The Office Action also contends that the term "a metal via" which is used in claim 10 is not substantially different from "a metal passage" cited in claim 1. Applicant respectfully disagrees with this objection. A via as used in the context of the present invention, i.e. as used in an electronics context, refers to a "vertical interconnect access" which is a plated through-hole that provides an electrical connection between two sides of a board or between different layers in the case of a multi-layered structure. To support this definition of "via", Applicant includes definitions from multiple sources included as Exhibits attached hereto. As will be further detailed below, neither Sekine nor Tsai disclose a structure in which a via is used as in the present invention.

Claims 1-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sekine. In view of the amendments made to claim 1, Sekine does not teach a passage through an antenna printed circuit board which transposes into a bond pad against and in direct contact with the

second side of the antenna printed circuit board, wherein the passage is in contact with the wall of the hole through the antenna printed circuit board. Further, Sekine does not have a bond wire connected between an electronic component and the central conductor 6 or the solder material 13-2. Although Figure 6 of Sekine discloses bond wires, the bond wires of Sekine extend between a chip 4 and a metal pattern on circuit substrate 3 and not on the base plate 1. Applicant asserts that claim 1 patentably distinguishes over Sekine or any other prior art or combination thereof and requests that the rejection be withdrawn.

Regarding claim 2, Applicant asserts that it is the combination of having a very short metal passage through the antenna substrate that transposes in a bond pad and a very short bond wire connecting said bond pad with the electronic component that achieves the advantages of the invention as recited in claim 2. Those advantages are not obtained with the structure of Sekine and are not obvious in view of Sekine.

Claim 3 has been amended and it is now clear that the conductive plate is provided on the second side with a recess for the bond pad, and that the electronic component is mounted on the conductive plate. The Office Action refers to an element 5 in figure 1. Applicant asserts that this characterization is incorrect, since element 5 is a cover plate and not an electrically conductive plate arranged against the second side of a substrate. It may be possible that the Office Action intended to reference ground plane 21 or ground plane 31 where metal patterns are provided with a recess for the central conductor 6 of the coaxial line. However, when amended claim 3 is read in conjunction with claim 1, it is clear that the combination of claimed features is not disclosed or suggested by Sekine. In Sekine, the metal patterns 31, 21 are not arranged as in the present invention on the second side of an antenna printed circuit board and spaced apart at a distance of a thickness of the bond pad. Moreover, the chip 4 is not provided on this ground plane, but on the electrically conductive base 1.

Regarding claim 8, the Office Action states that Sekine teaches that the periphery of the passage substantially corresponds with the width of the power supply line. Applicant asserts that this characterization is not true. From Figure 1 for example, it is clear that the central conductor 6 is many times thinner than the width of the metal patterns of the planar antenna. In order to further clarify claim 8, the periphery being calculated as the diameter of the passage multiplied with π has been added.

Claims 10-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai. However, it is believed that Tsai is not correctly interpreted and Applicant traverses the rejection.

According to the Office Action, element 162 in Figure 1 of Tsai would be an electronic component. Applicant asserts that with a careful reading of Tsai, this is incorrect. Element 162 is a metal block of a hinge base 16 of a computer, see also Figure 4 of Tsai, which shows the hinge base.

Moreover, the Office Action characterizes element 222 as a metal via. Applicant asserts that this cannot be so. Element 222 is a circular aperture. As explained in column 2, lines 37-42 of Tsai, the cable 28 (a coaxial cable) comprises a conductive core wire 282 and a conductive ground shield 284 around the core wire 282. The core wire 282 is inserted through the second surface 223, the aperture 222 and the first surface 221 and is soldered to an inner extreme point 242 of the antenna 24 on the first surface 221. The ground shield 284 connects with the metal sheet 26 on the second surface 223 near an inner extreme point 262 of the metal sheet 26. Therefore, the circular aperture 222 is not a metal via and does not transpose in a bond pad.

In addition, the Office Action states that element 284 is a bond pad. However, element 284 is the conductive ground shield of the coaxial cable 28.

The Office Action also contends that there is a metal bond wire (connection between 284 and 262, Figure 3) between the electronic component and the bond pad. As mentioned above, element 284 is not a bond pad. Moreover, element 262 is not an electronic component, but merely a metal sheet for forming the ground plane of the antenna.

Applicant further notes that there is no electronic component mounted on the second side of the printed circuit board 22. There is an electrical wire 282 passing through aperture 222 and connected with the coaxial cable 28. It is this coaxial cable 28 that is connected to an electronic component inside a computer. This is a fundamentally different structure compared with the present invention where an electronic component is mounted on the second side 223 of the printed circuit board.

In view of the arguments and clarification provided above, Applicant asserts that claim 10 is new, novel and non-obvious. Moreover, claim 10 has been amended to recite that the bond pad is in direct contact with the antenna printed circuit board. Applicant respectfully requests that the rejection be withdrawn.

Regarding claims 11-16, the same amendments have been made as to claims 2-9. As claims 1 and 10 are allowable when Tsai is correctly interpreted, the features of claim 11-16 are not disclosed or obvious in view of Tsai and Applicant asserts that these claims are also allowable.

A speedy and favorable action in the form of a Notice of Allowance is hereby solicited. If the Examiner feels that a telephone interview may be helpful in this matter, please contact Applicant's representative at (612) 336-4728.

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725.

Respectfully submitted,

MERCHANT & GOULD P.C.

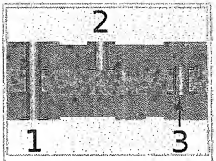
Dated: 9/2/10

By: _____
Gregory A. Sebald
Reg. No. 33,280
GAS/krn

Via (electronics)

From Wikipedia, the free encyclopedia

Via stands for "Vertical Interconnect Access" which is a vertical electrical connection between different layers of conductors in printed circuit board design. **Vias** are pads with plated holes that provide electrical connections between copper traces on different layers of the board. The holes are made conductive by electroplating, or are filled with annular rings or small rivets. High-density multi-layer PCBs may have **microvias**: **blind vias** are exposed only on one side of the board, while **buried vias** connect internal layers without being exposed on either surface. **Thermal vias** carry heat away from power devices. They are typically used in arrays of about a dozen vias.

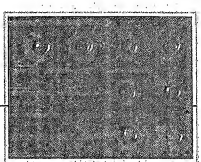


Different types of vias:
(1) Through hole.
(2) Blind via.
(3) Buried via.
The grey and green layers are non-conducting, while the thin orange layers and vias are conductive.

In integrated circuit design, a via is a small opening in an insulating oxide layer that allows a conductive connection between different layers. A via on an integrated circuit is often called a through-chip via. A via connecting the lowest layer of metal to diffusion or poly is typically called a "contact".

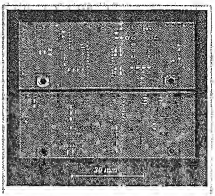
See also

- Printed circuit board (PCB)
- Through-hole technology (THT)
- Surface-mount technology (SMT)



Plated-through holes, in this section there are eight on a multilayer board (hugely magnified)

Double layered plating in CAD. Vias makes EDA placement possible.
Bottom layer - Red
Top layer - Blue



Vertalen
Woorden (Hoofdpagina)
Tekst
Meest vertaald

Ontspanning
Puzzelwoorden
Woordspellen
Rijmwoordenbrek

Synoniemen
NL | DE | EN | ES | FR

Werkwoorden
Werkwoorden vervoegen

Spelling
Spellingatlas
Goed en Fout
Spellingcontrole

Varia
Dialecten
Encyclopedie
Woordenboek Nederlandse taal
Symbolen en ALT-codes
Tellen in andere talen
Thamawoordenboeken
Thai site in English

Taalportalen
NL | DE | EN | ES | FR

De website
Contact | Privacy

NL-EN EN-NL

Toon alle themawoordenboeken

Elektrotechniek (EN-NL)

228 woorden met de letter **V:** Vorige 1 2 **3** 4 5 Volgende

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z Overig

very high density plasma

EN: very high density plasma
NL: *plasma van zeer hoge dichtheid*
Definitie EN: A plasma whose pressure exceeds the mechanical strength of solid material when its temperature is high en for thermonuclear reactions to occur.

very high frequency

EN: very high frequency, metric wave, VHF
NL: *metrieke golf, VHF, zeer hoge frequentie*
Definitie EN: a Federal Communications Commission designation for a frequency in the band from 30 to 300 MHz,corresponding to a metric wave between 1 and 10 m

very low frequency

EN: very low frequency, VLF
NL: *zeer lage frequentie;VLF*
Definitie EN: a Federal Communications Commission designation for a frequency in the band from 3 to 30 kHz,correspond to a myriametric wave between 10 and 100 km

vestigial sideband

EN: vestigial sideband, VSB
NL: *VSB, asymmetrische zijband, restzijband*
Definitie EN: a sideband in which some of the spectral components,in general those corresponding to the highest frequen the modulating signals,are greatly attenuated

vestigial sideband

EN: vestigial sideband
NL: *restzijband*
EN: VSB
NL: *asymmetrische zijband*
Definitie EN: a sideband in which some of the spectral components,in general those corresponding to the highest frequen the modulating signals,are greatly attenuated

vestigial sideband emission

EN: vestigial sideband emission
NL: *restzijbandemissie*
Definitie EN: a transmission where frequency components below the visual carrier are substantially suppressed

VFD

EN: VFD, vacuum fluorescent display
NL: *vacuüm-fluorescentiedisplay*
Definitie EN: a light-emitting triode utilizing fluorescent phosphors which can be used in alphanumeric display panels

VG

EN: VG
NL: *spraakgroep*
Definitie EN: the designation given to the encoded channels of a pulse code modulation span line

VHF

EN: VHF
NL: *zeer hoge frequentie*
EN: very high frequency
NL: *metrieke golf*
Definitie EN: a Federal Communications Commission designation for a frequency in the band from 30 to 300 MHz,corresponding to a metric wave between 1 and 10 m

VHF channel

EN: VHF channel
NL: *VHF-kanaal*
Definitie EN: one of the 6-MHz television channels designated by the numbers 2 through 13

via

EN: via, via hole, feedthrough
NL: *via-gat, via*
Definitie EN: a plated-through hole used as a through connection, but in which there is no intention to insert a componen lead or other reinforcing material

vibrating batteries

EN: vibrating batteries
NL: *oscillerende batterijen*
Definitie EN: the batteries that cause a phone to vibrate instead of ringing

vibration test

EN: vibration test

Printed Circuit Design Glossary

Any glossary is bound to include mistakes of fact, emphasis, typography and omission. Please tell us about those you notice - you can cut and paste sections to e-mail us your wisdom.

If you click on these initial or other links and they don't work, probably the whole file is not yet loaded. Just wait a while, or until the busy indicator disappears, and try again.

You can use the Browsers Find facility in the usual way to find things if you prefer.

Symbols A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

Symbols

274D

274X
Casual names for an extended RS-274D and RS-274X used to define Gerber Photoplot file format.

3rd Angle projection
Representation of a 3 dimensional object by means of three orthogonal views from the Front, Side & Top.
See also Isometric Projection.

A

Analogue

Designs and parts that use continuously variable voltage, current, resistance etc. to represent real world values. e.g. a voltage of 1 Volt might represent freezing point, and 2 volts boiling point. You might set switching thresholds for a thermostat using a comparator.
See also Digital.

Annotation
Adding notes to a schematic, in particular filling in the legends describing a component (e.g IC2, R45, C3) and labelling the pin tags with the actual pin numbers used in the PCB, allowing for gate allocation, equivalent pin swapping, and similar that may take place during PCB layout.

Annular Ring
A Pad Shape consisting of a doughnut shape. Uses include
- A drill centre mark.
- On a Powerplane, to provide isolation for a drilled hole through it's centre. Plotting for powerplanes is performed as a NEGATIVE - draw where you do NOT want copper. Thus the ring generates an isolated island. The inner section must provide normal electrical clearance plus the tolerance on drill position and layer registration. Many manufacturers prefer an annular ring to an isolating disk because it prevents a void at the drilled hole which might introduce through-plating difficulties.

Antenna
A structure to transmit or receive electromagnetic radiation. In PCB design tracks may be deliberately designed in lines, loops or spirals to provide such function (e.g. Key-fob transmitters). They may also be created unintentionally on high speed signals and generate interference, or on sensitive signals that makes a circuit sensitive to external electromagnetic radiation.
See also EMC.

Application
Software that performs some end-user task.

API
Application Programmers Interface - the facilities and controls offered to applications by the operating system and any add-ons. Normally includes Disk file handling, Timer services, Screen (window) painting, Keyword and Mouse sensing, Network access etc.

Astable
A circuit element or wiring of gates that keeps changing states, usually at a regular rate to provide a 'clock' signal.
See also Bistable and Monostable.

ATE
See Automatic Test Equipment.

Automatic Test Equipment
A test jig designed to test and diagnose finished and/or bare PCBs. See also Bed of Nails and Test Point.

Automatic Placement
An automatic facility for Placement. You will need to provide fixed positions for connectors, a board outline, and possibly other constraints for height above board, pairing of components such as decoupling capacitors, and the like.

Automatic Routing
A program to take a Rats Nest and alter the connections paths to attain a pattern without crossing tracks, going outside the board area, entering disallowed areas, etc. Where necessary signals will move from layer to layer by changing sides at introduced VIAs. Surface mount pads needing to connect to a powerplane have appropriate stalks and VIAs introduced.
Many styles of routing exist. Vutrax supports 3 styles
1. Basic: A router that basically lays in right angled tracks, vertical on one layer and horizontal on another. Can lay in tracks very quickly and neatly, but will not reach 100% completion. Vutrax includes the Basic router 'Autotrack' which can perform Bus Routing - a great time saver - Track Necking, and various other explicit activities not present in more advanced routers.
2. Rip-up: A more sophisticated router including the capabilities of Basic routing, but which can remove and reroute signals to accommodate subsequent signals that can not be routed, and can lay track paths in very complex and imaginative ways when required. These routers can often attain 100% completion. Vutrax includes the Rip-up Router Varoute.
3. Shape-Based & Other Schemes: Advanced routers (with price and system demands to match) that will reach 100% completion if the layout reasonably allows it. These routers are often provided as third party

Track Impedance
The effective impedance of a track as determined by its width and association with other tracks and any groundplane. See also Stripline.

Track Necking
Narrowing of a PCB track to fit through a small space, for example to go between component pins. Wide tracks have advantages in being less likely to be manufactured with discontinuities, less likely to crack over time, carry current with less heating, and therefore less stress on adhesives. Thus it is common to narrow a track only where necessary. See Track Width.

Track Routing
Arranging the connections in a Rats Nest to achieve the required interconnections with no shorts or inadequate clearances. See Routing.

Track Width
The width of a Track on a PCB is determined by a combination of factors:-

- Must be wide enough that manufacturing is able to reliably produce a track with no breaks.
- Must be narrow enough to accommodate the density of signals required on the design.
- Must be wide enough to carry the necessary current without excessive heating - see Track Current Capacity.

Track Shuffling
Mass moving a selection of Tracks, usually to pack them with minimum clearance to make room for further connections through the same area of the PCB.

Track Pattern
Often groups of Tracks are routed in a similar pattern. Vutrax offers a feature to automate this process. See also Bus Routing

Track Current Capacity
This is a quite complex area - there is a treatise on it at the Vutrax web site. See also Track Width.

Transistor, Bipolar
A transistor where the current between Emitter and Collector is determined by a smaller current applied to the Base (i.e. a current amplifier).

Transistor, FET
A Field Effect Transistor - the current between Source and Drain is determined by the electrical field from an isolated Gate (i.e. voltage control).

Transmission Line
On PCBs, a term referring to designing track layout to have an accurately defined Track Impedance, often consisting of a pair of conductors (either differential or signal and return) running in parallel.
See also Stripline and Microstrip

TTL
Transistor Transistor Logic was the initial implementation of the 74xxnnn series logic (TTL being the form with xx omitted).

U

UNIX

An operating system dating back to 1970 still widely used for Networks of various sorts (most Internet infrastructure machines use some form of UNIX) and increasingly as a personal operating system. It is designed to be secure and extremely reliable - systems can run continuously for years.
Available for a wide variety of processors, but limited in acceptability until recently because of lack of cooperation between competing development companies
A graphical front-end X-Windows is available.
See also Linux.

URL
Uniform Resource Locator - the textual form of addresses on the Internet. Note that separators are always '/' rather than '\'. e.g. the Vutrax web site has the URL

```
                http://www.vutrax.co.uk/index.htm
Protocol:       xxxx
Internet Site:      xxxxxxxxxxxxxxx
File name (can include directories):  xxxxxxxx
```

V

Vector Image

An image stored as a series of drawn lines. As such they can be scaled up and down without distortion, and easily manipulated to alter positions of items.
Modern display technology displays images using Bit Image techniques.
Conversion of a Vector image to a Bit Image at a chosen scale is easy. Once in this form conversion back to a vector image, or changing of scale, is a slow and unpredictable process.
Examples of Vector Images are Vutrax and AutoCAD DXF graphics formats.

VIA

A hole drilled through the board that is then plated, to provide selected connections between traces and/or Groundplane on different layers (or on Double Sided board, just the two sides).
Some low cost or ad-hoc manufacturing processes do not provide the plated-through hole (which is difficult to manage without use of horrid chemicals and complex processing) and instead 'pin through' necessary connection, or arrange for layer changes to occur at components that can be soldered on both sides.
See also Laser VIA, Buried VIA and Blind VIA.

VIA, Laser
A VIA produced by laser burning/evaporating holes. Such VIAs can be very small, and Blind VIAs can be produced in the same pass as through board VIAs by providing reflective copper at the 'deepest' layer.

VIA, Blind
A VIA that appear on one surface of a multilayer PCB, but stops part way through. PCBs may use a variety of Blind and Buried styles to attain higher